

FIG. 1

F/G.2

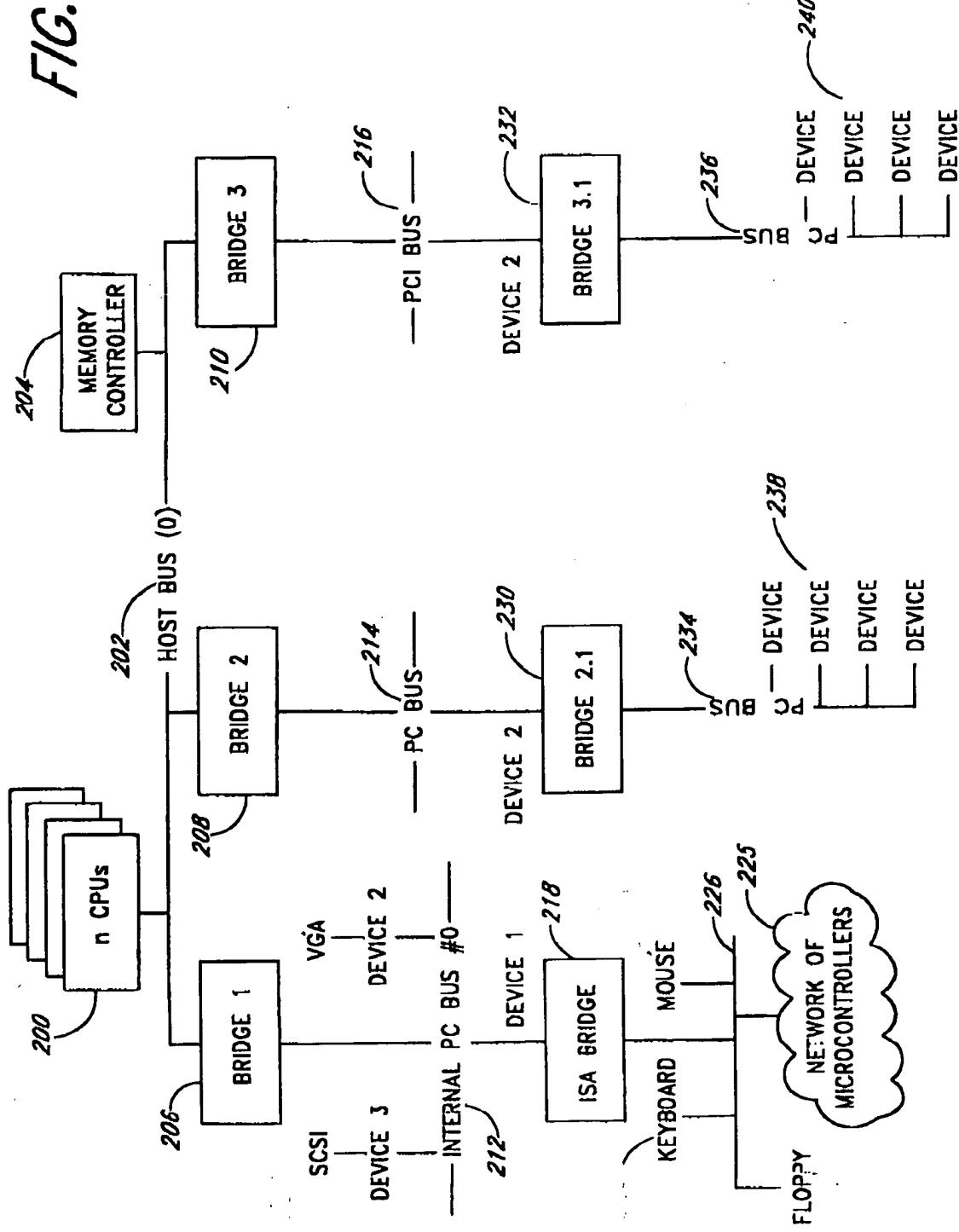
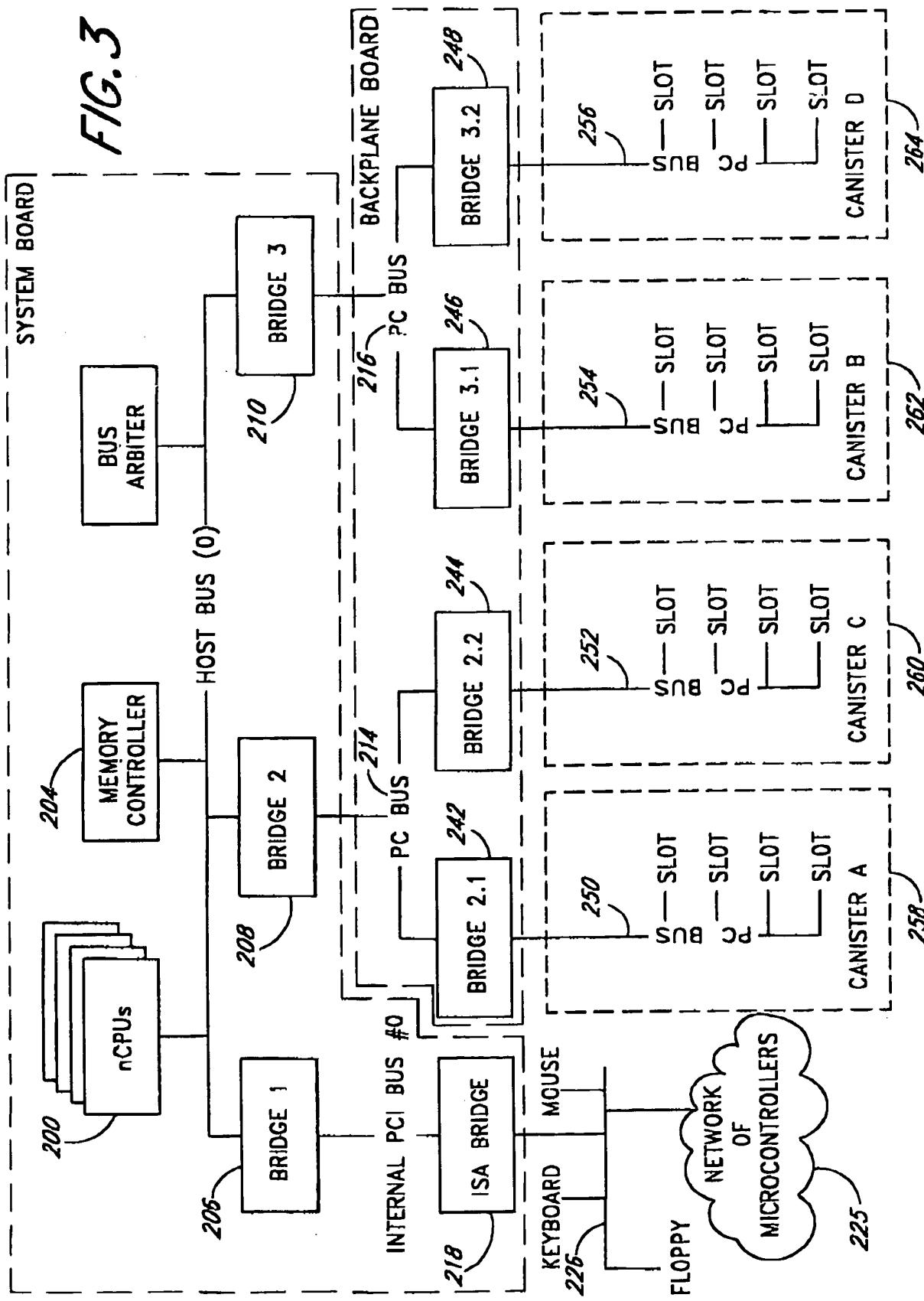


FIG. 3



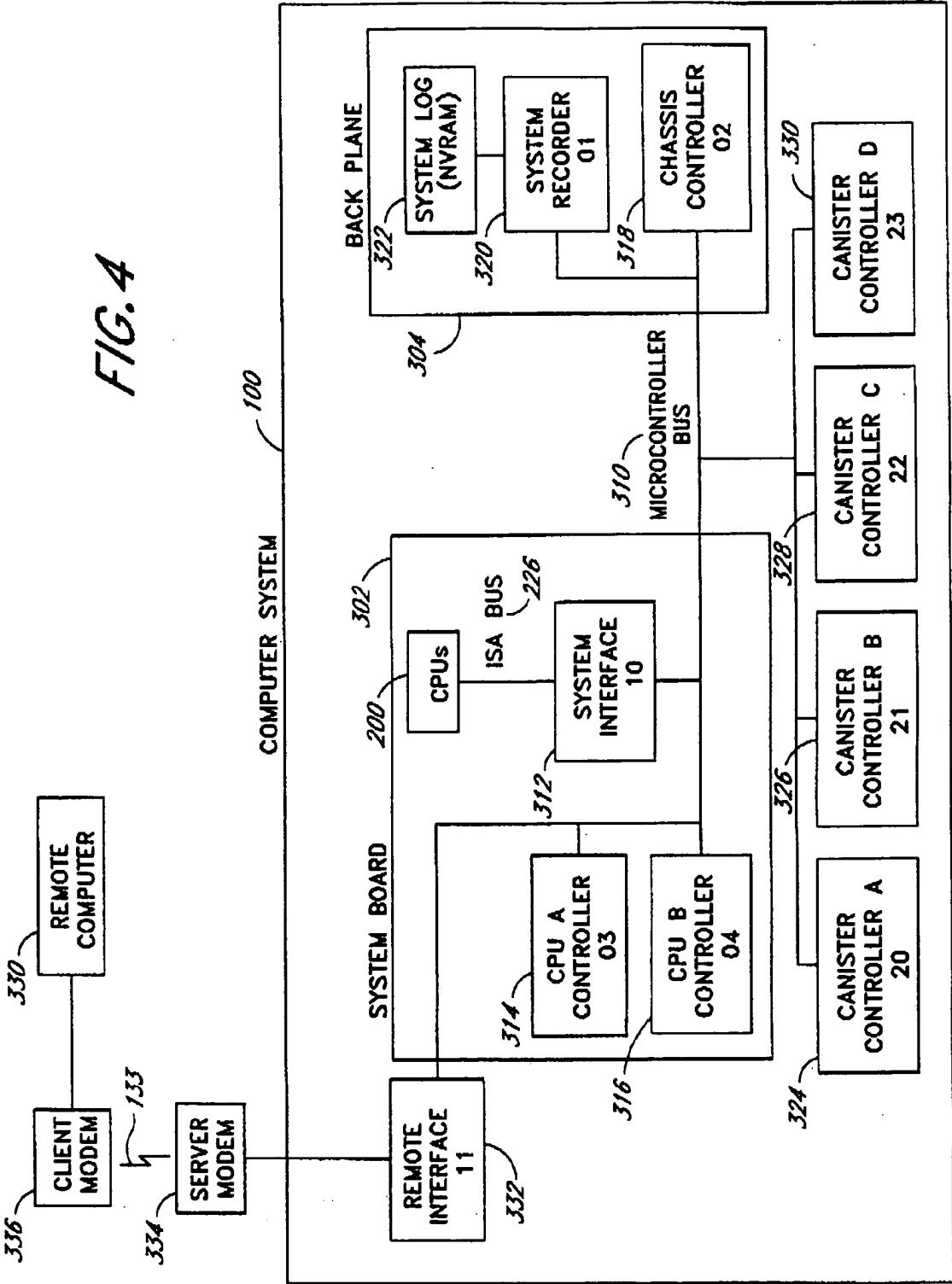
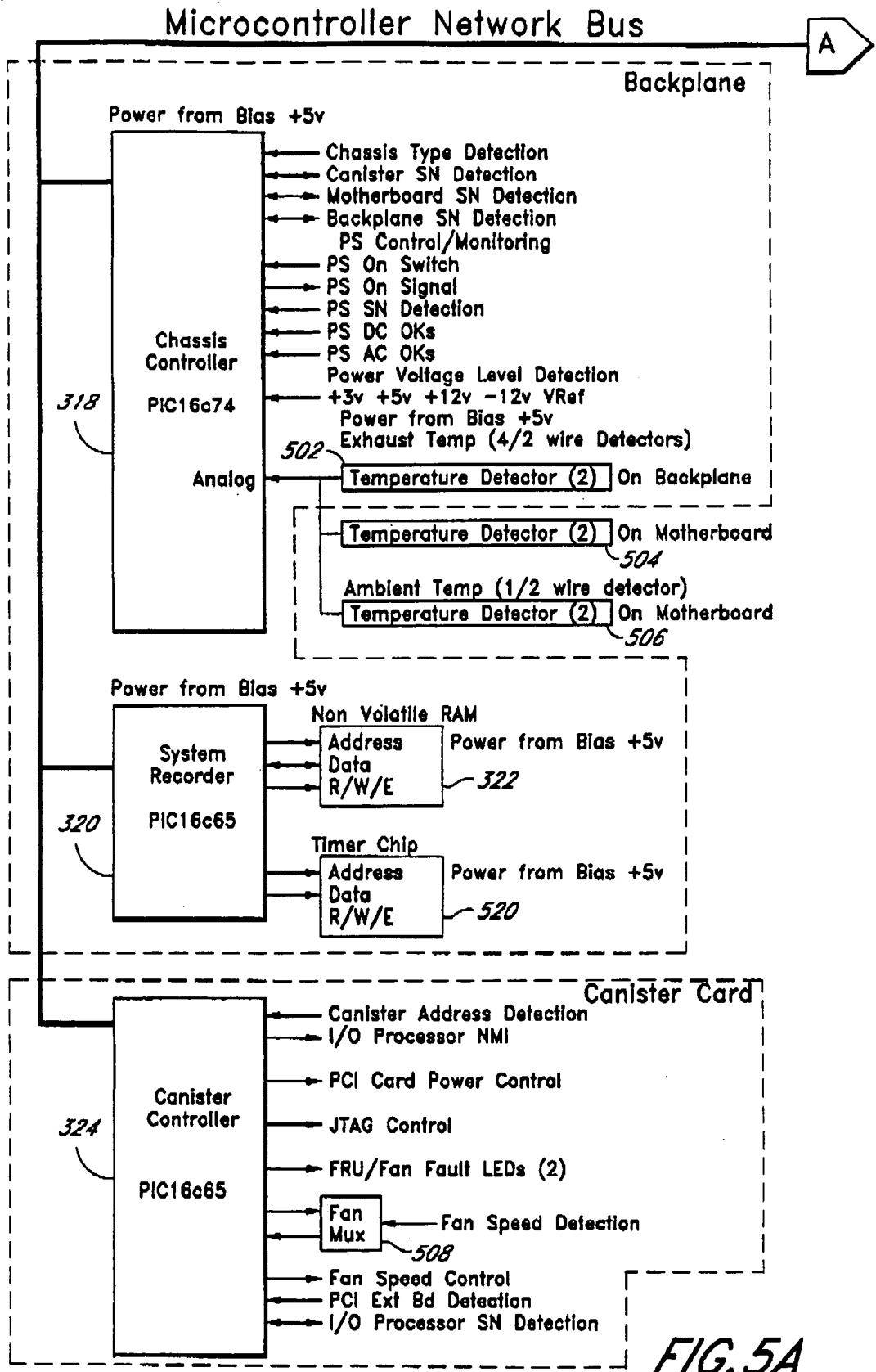
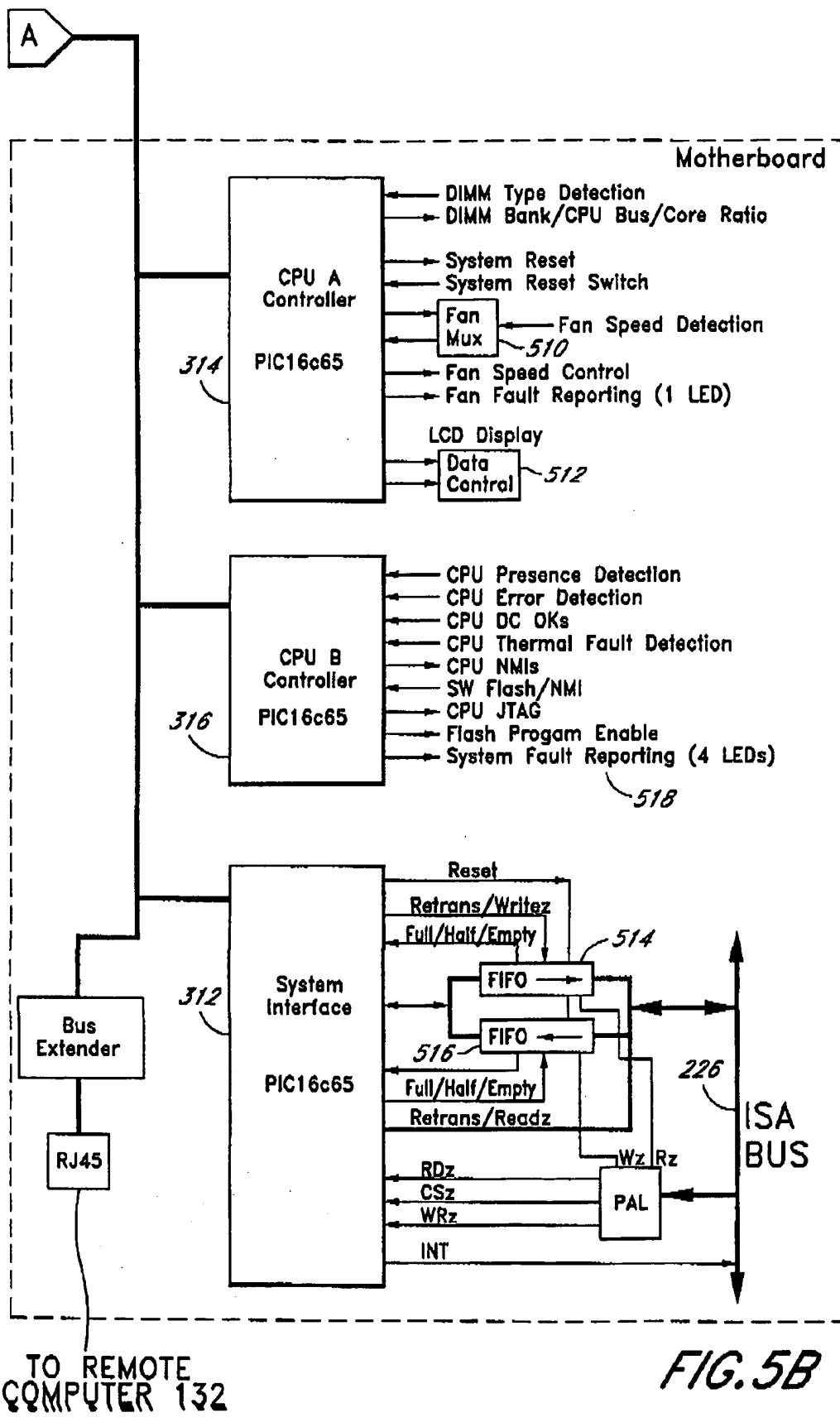


FIG. 4



0000000000000000



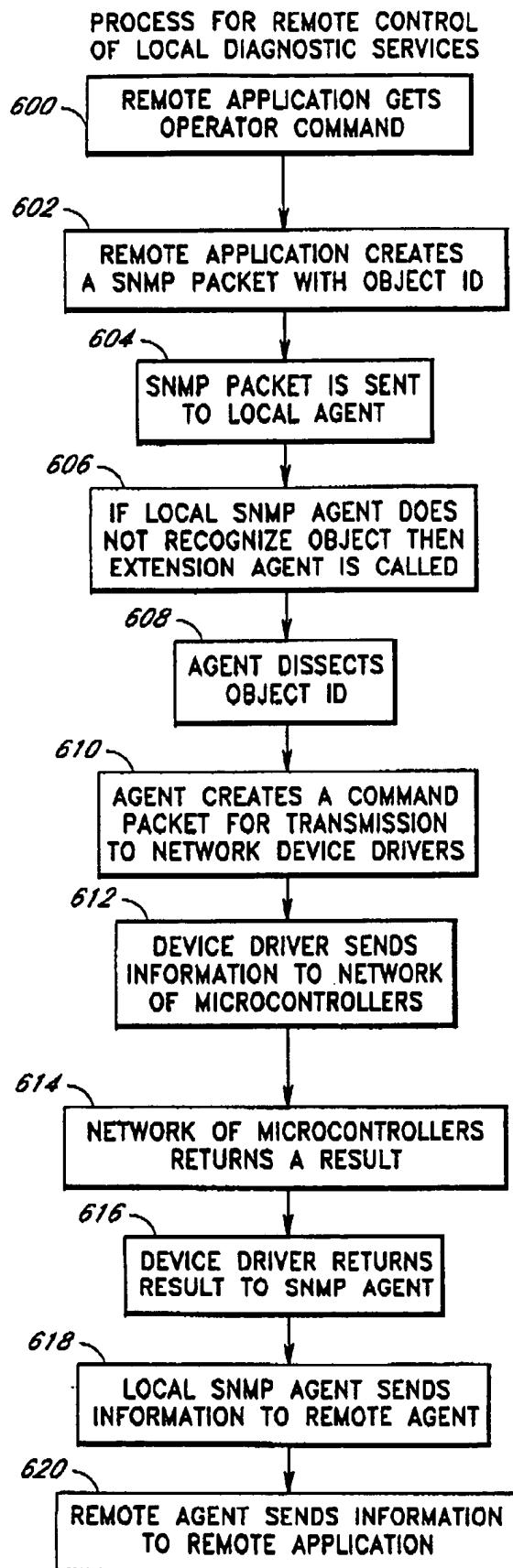


FIG. 6

ISA TO MICROCONTROLLER BUS INTERFACE

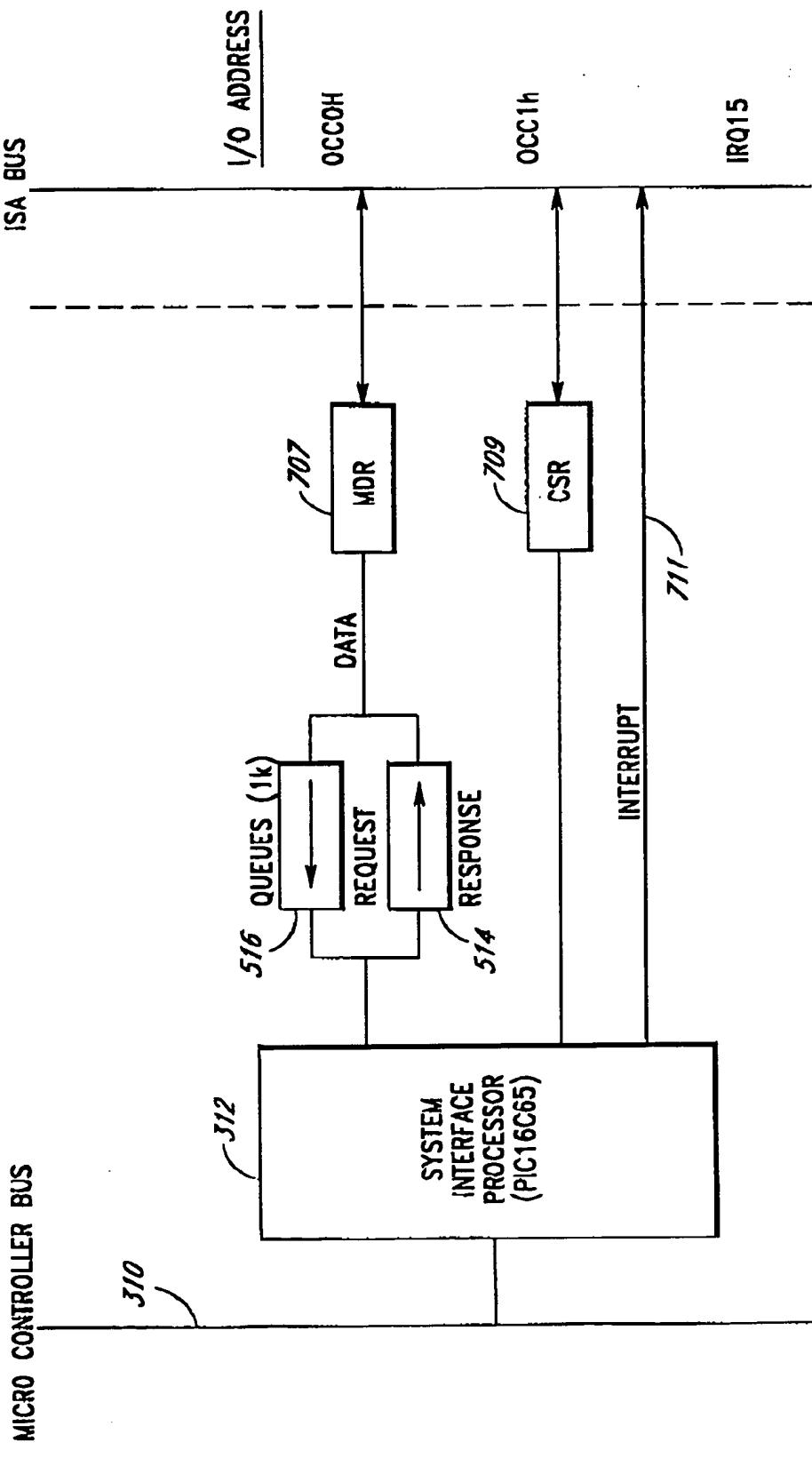


FIG. 7

MASTER TO SLAVE COMMUNICATION

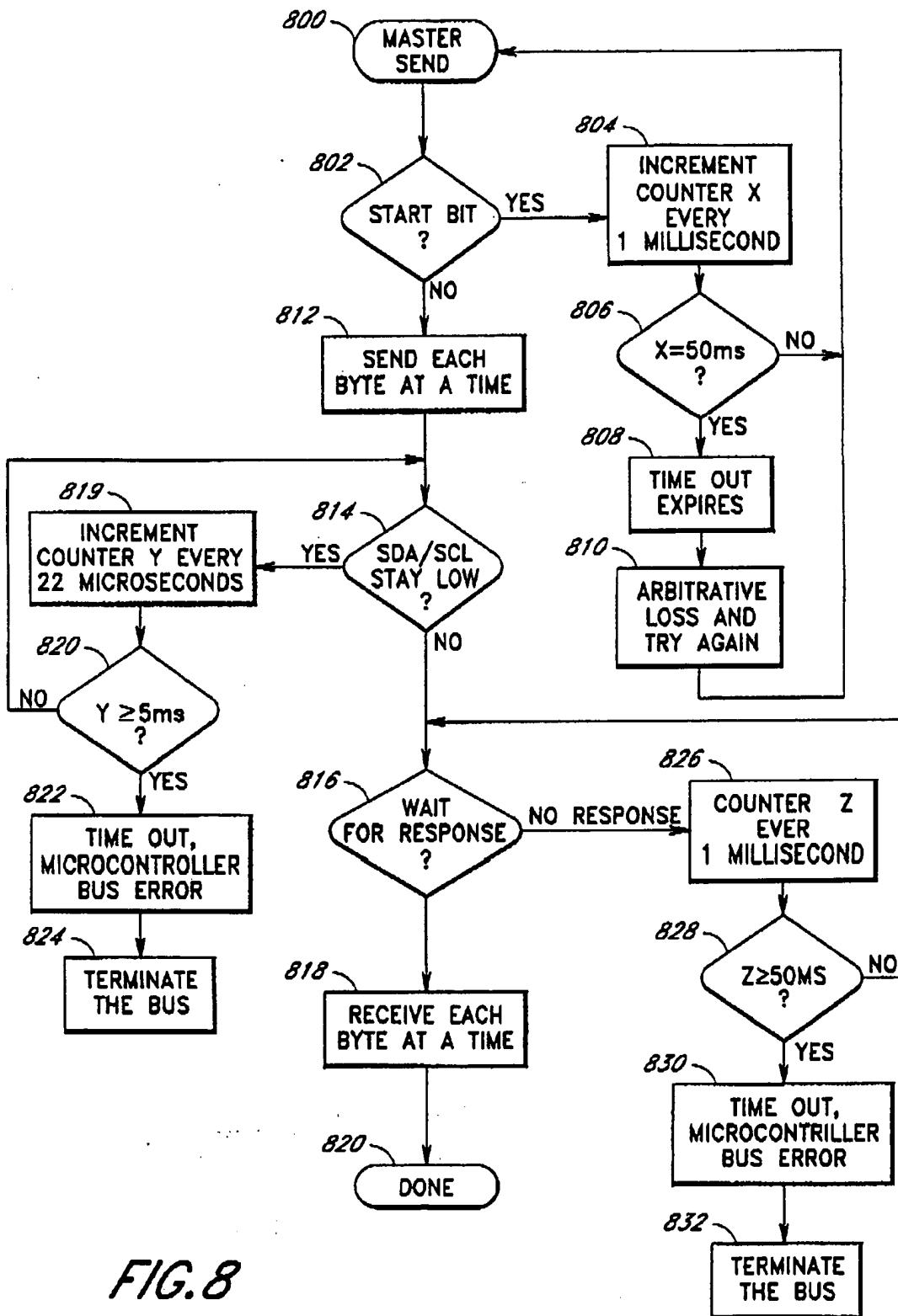


FIG.8

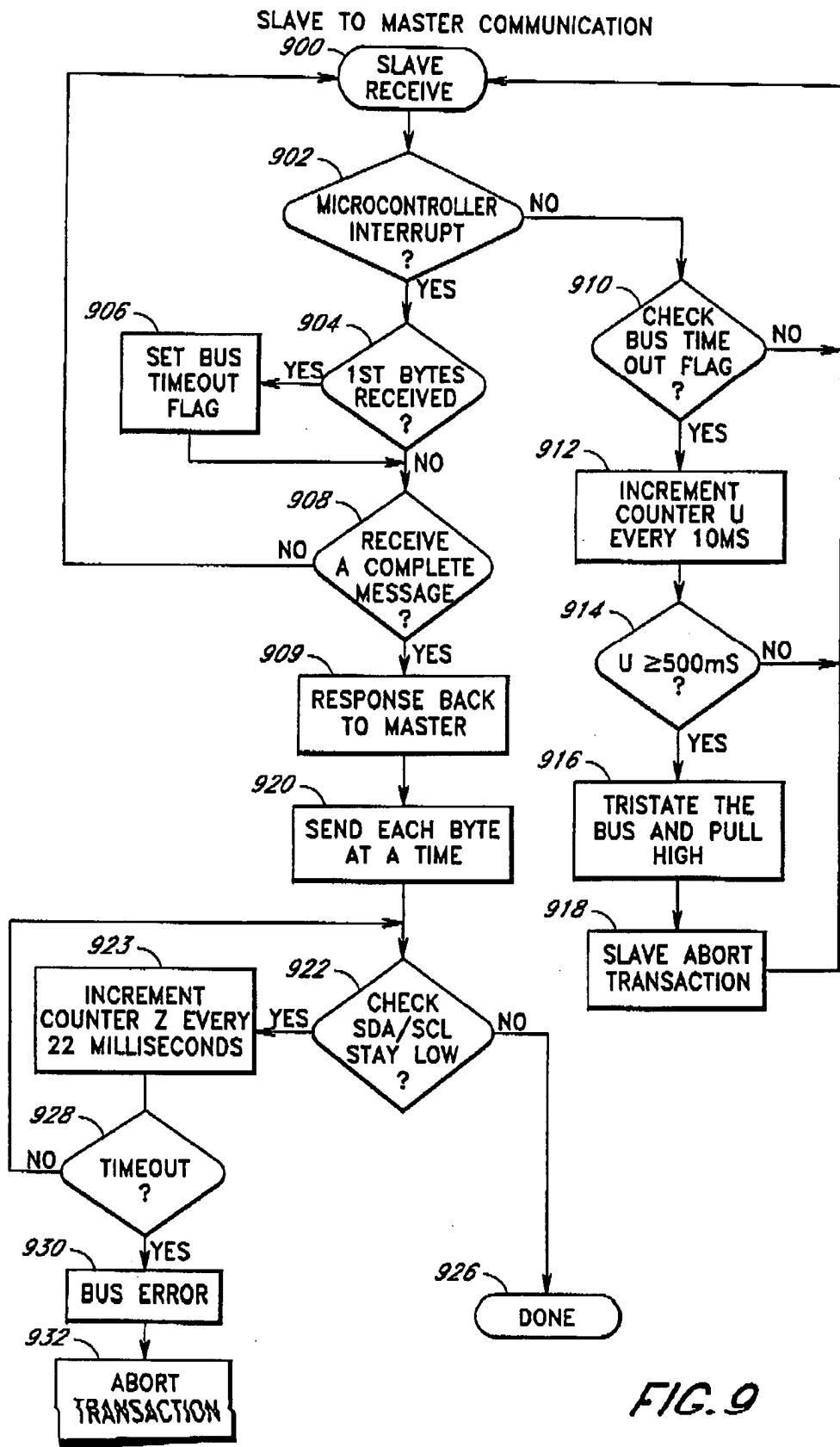
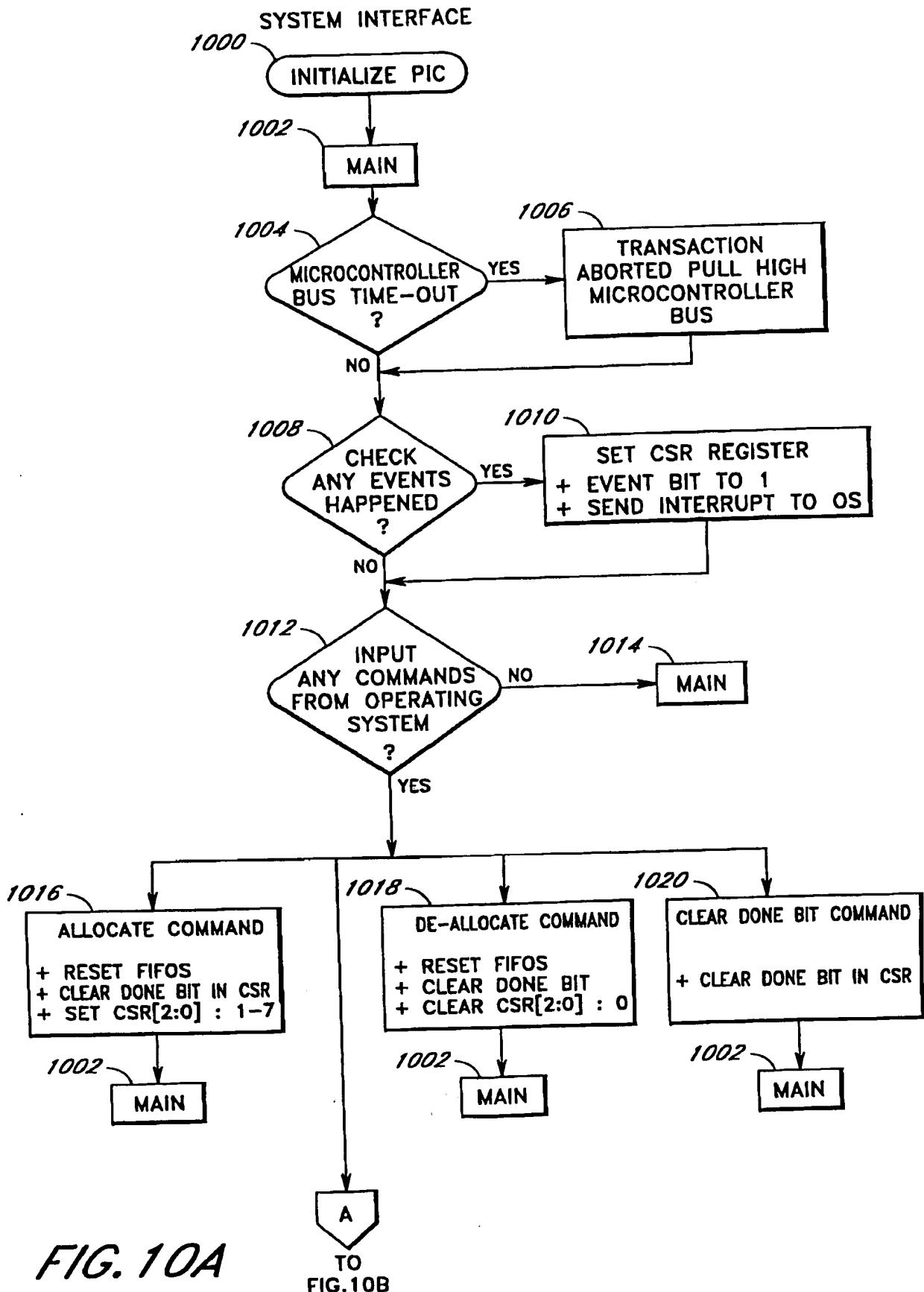


FIG. 9



SYSTEM INTERFACE (CONTINUED)

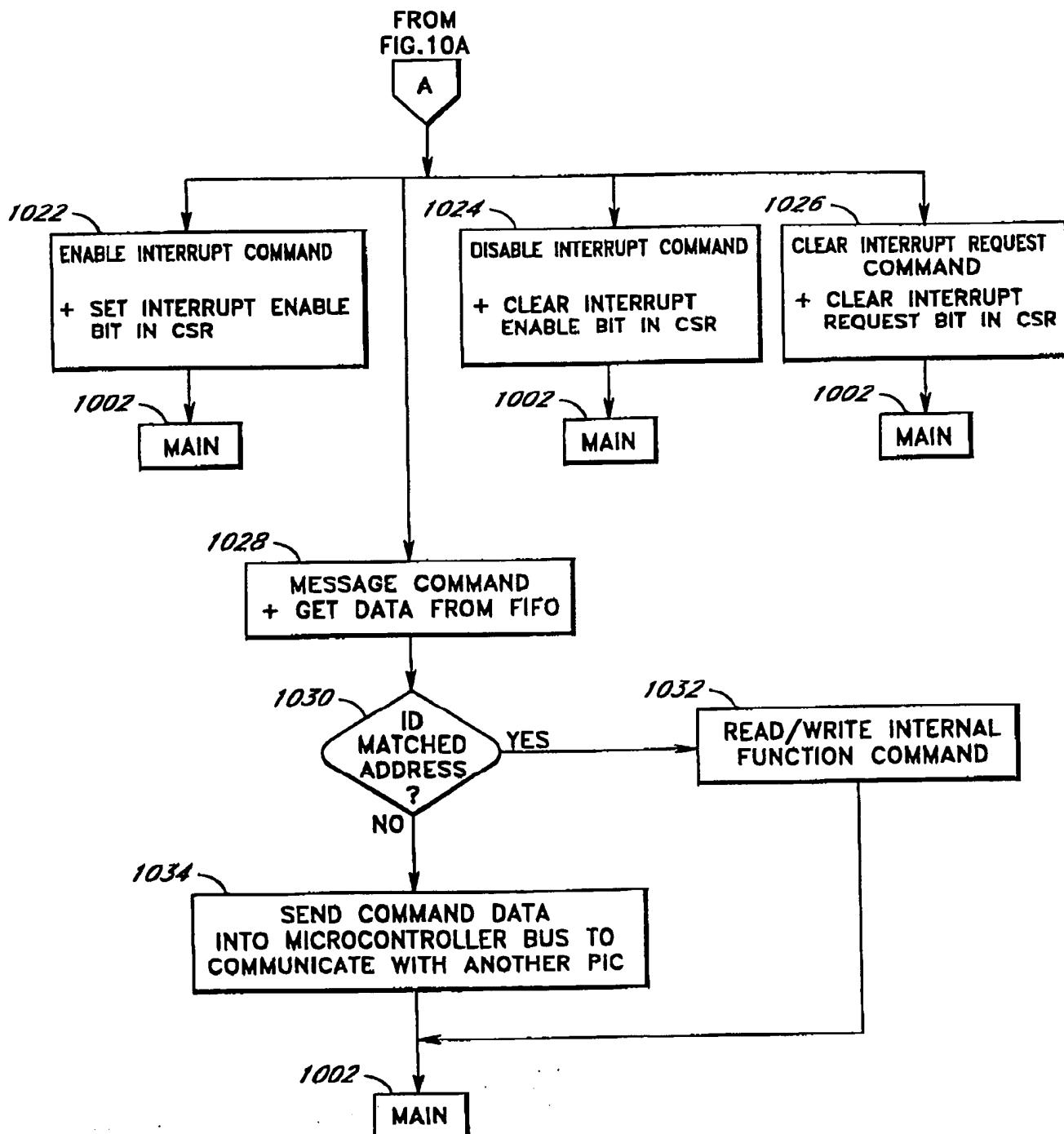
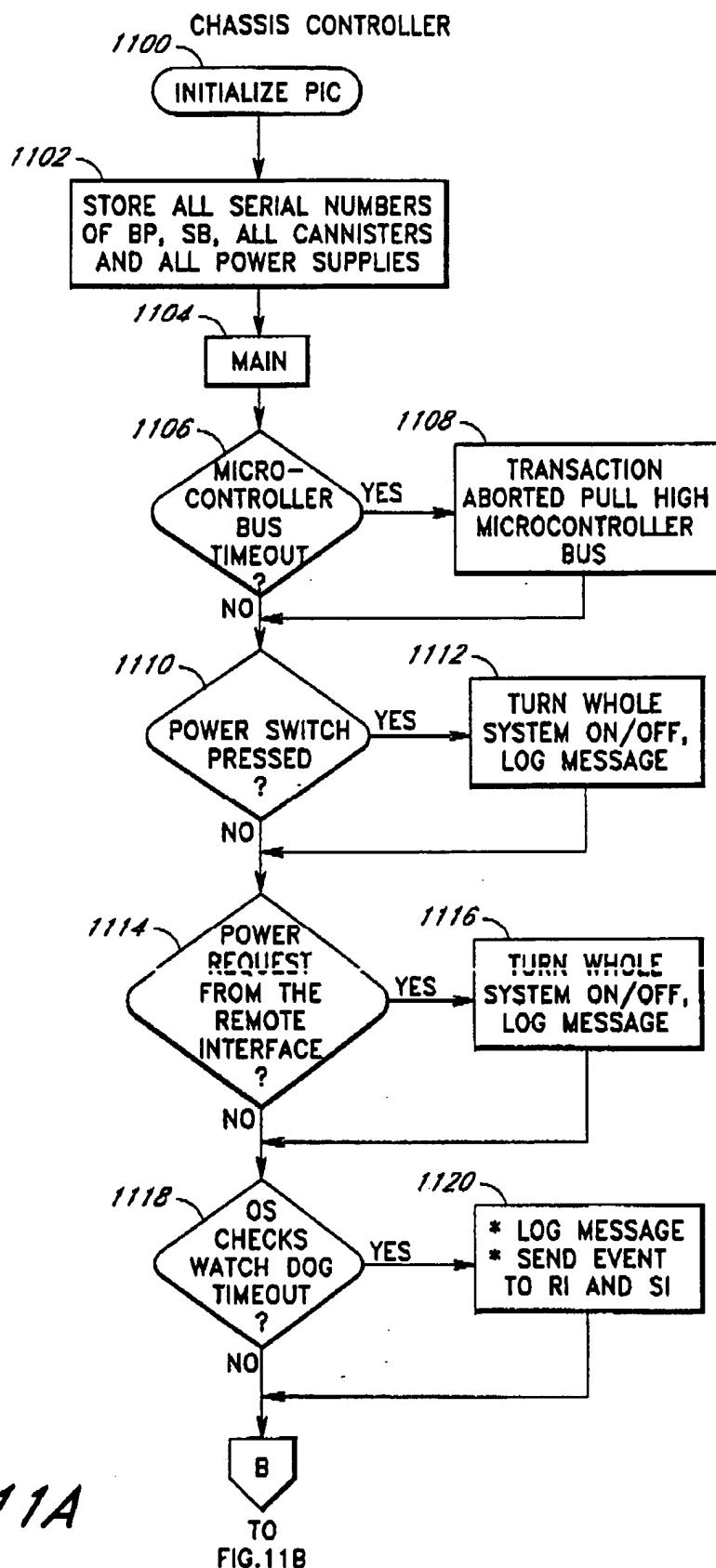


FIG. 10B



CHASSIS CONTROLLER (CONTINUED)

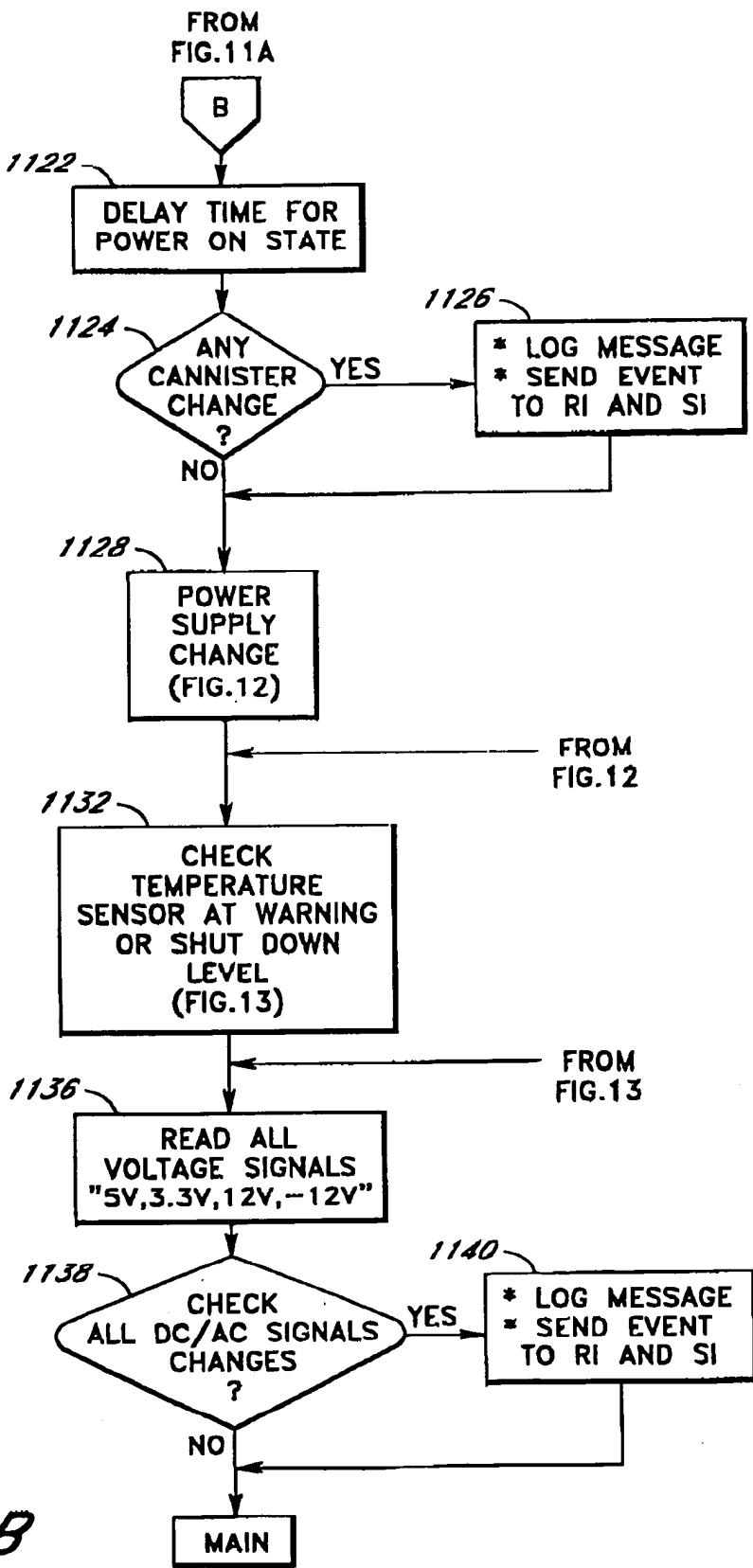


FIG. 11B

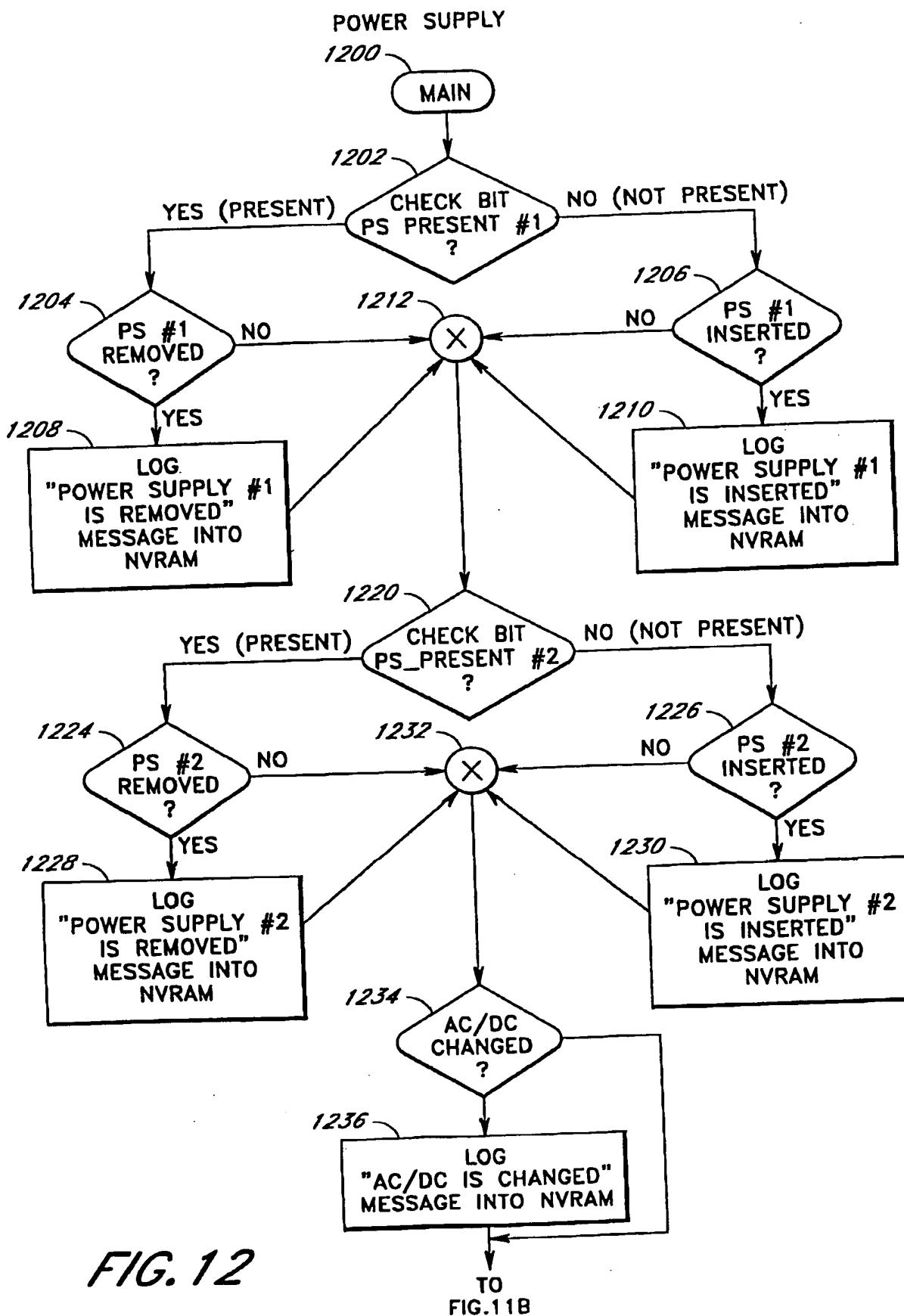


FIG. 12

TO
FIG.11B

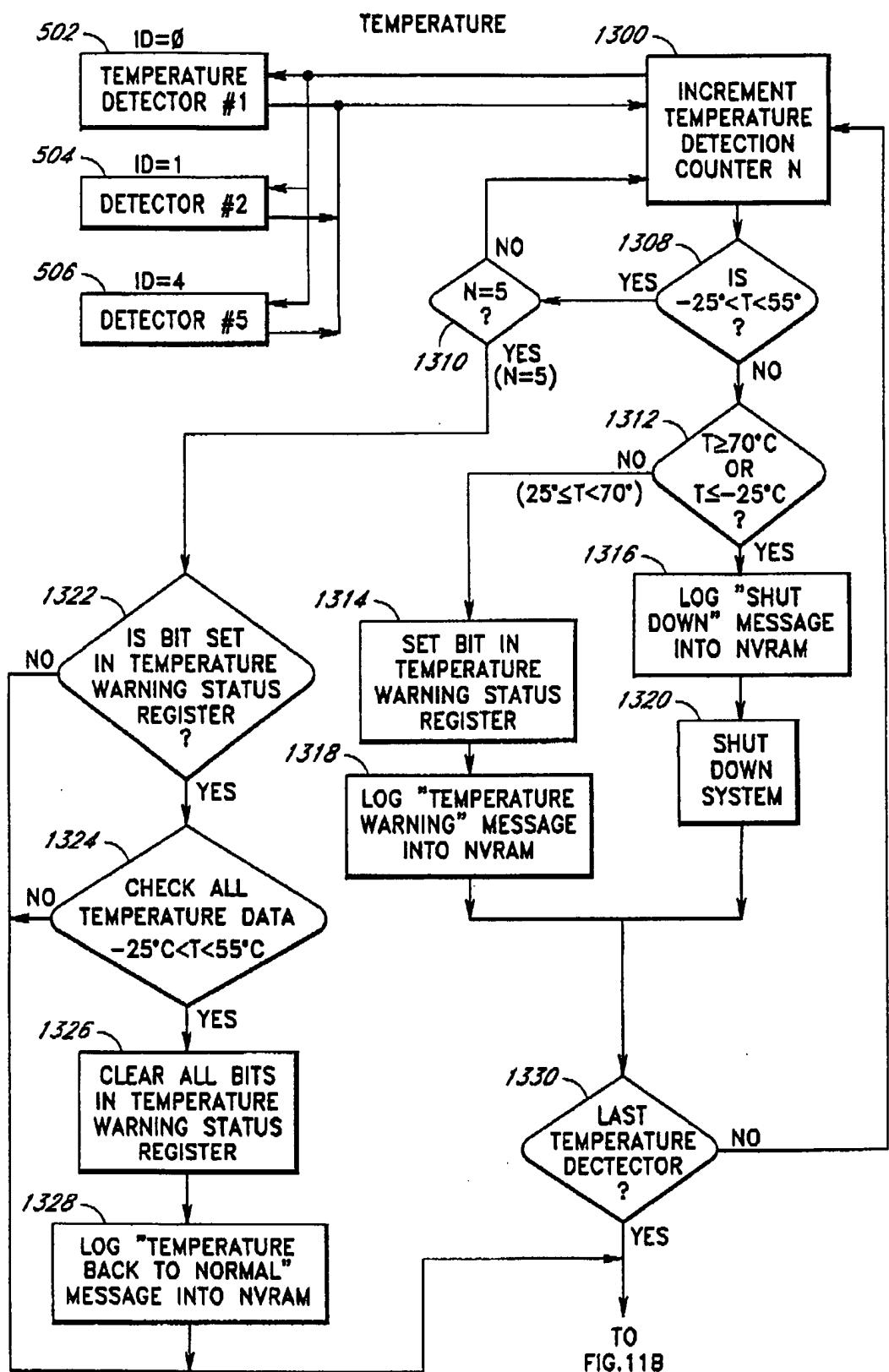
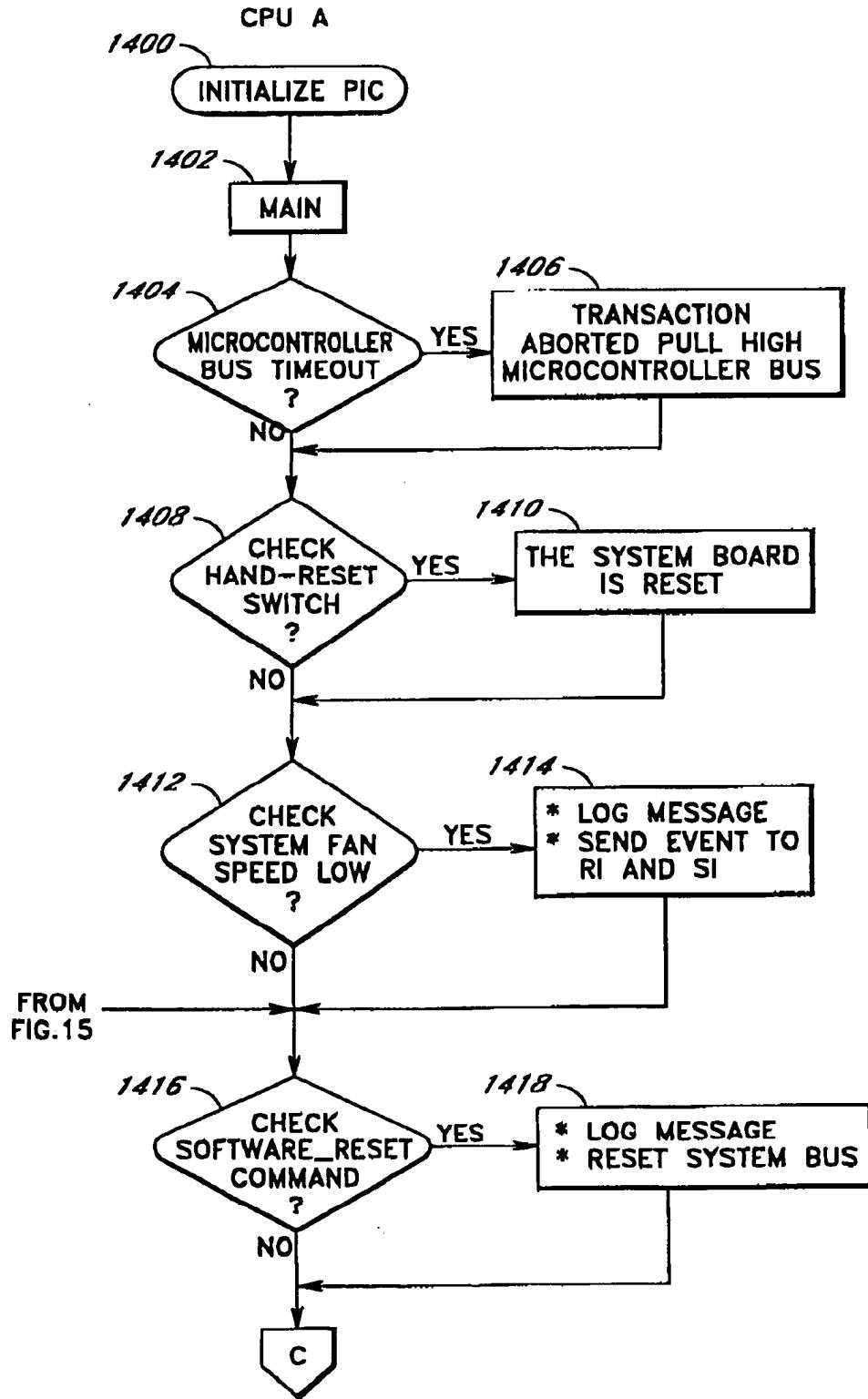


FIG. 13



CPU A (CONTINUED)

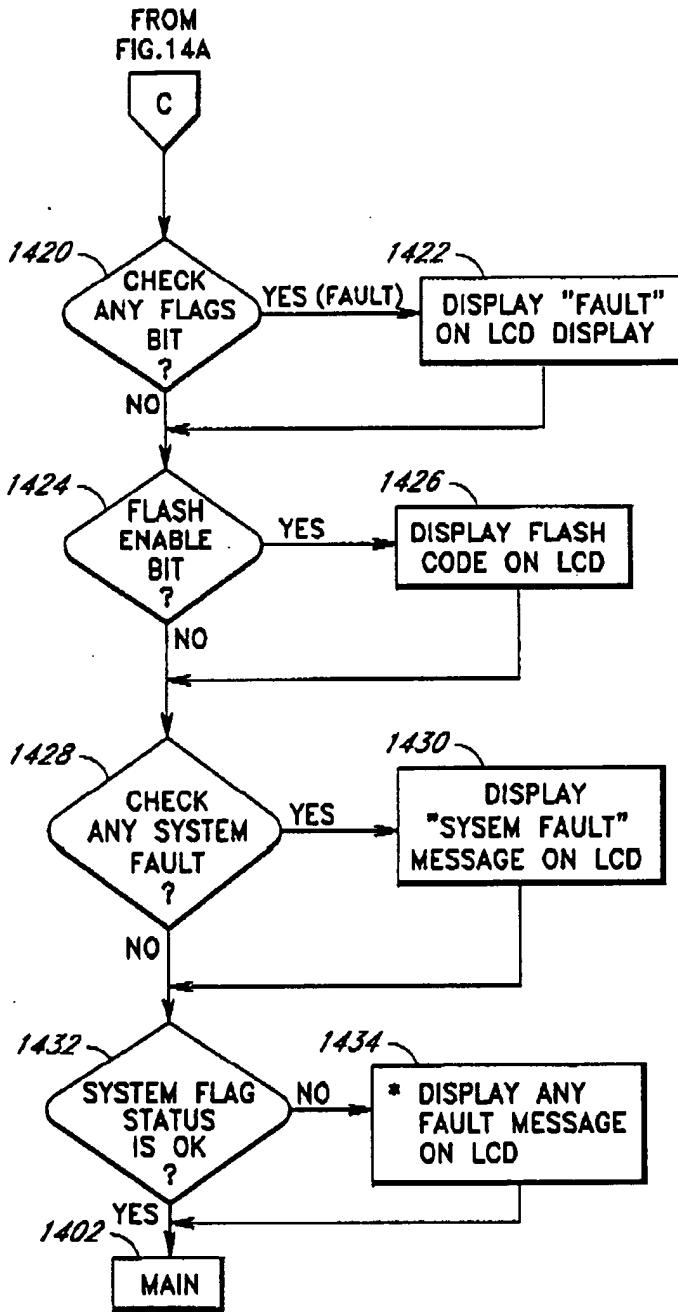


FIG. 14B

03942402 - 4006152

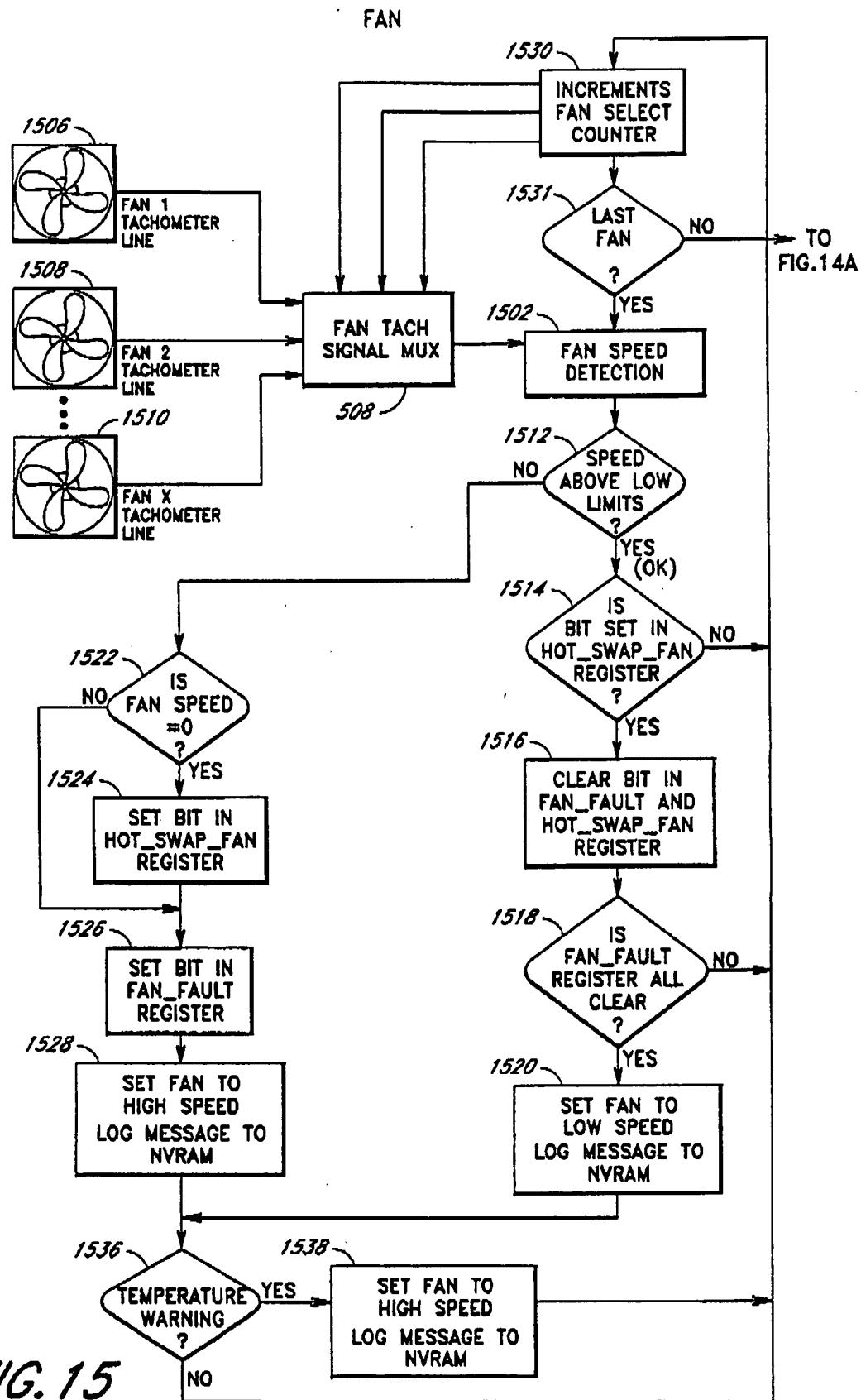


FIG. 15

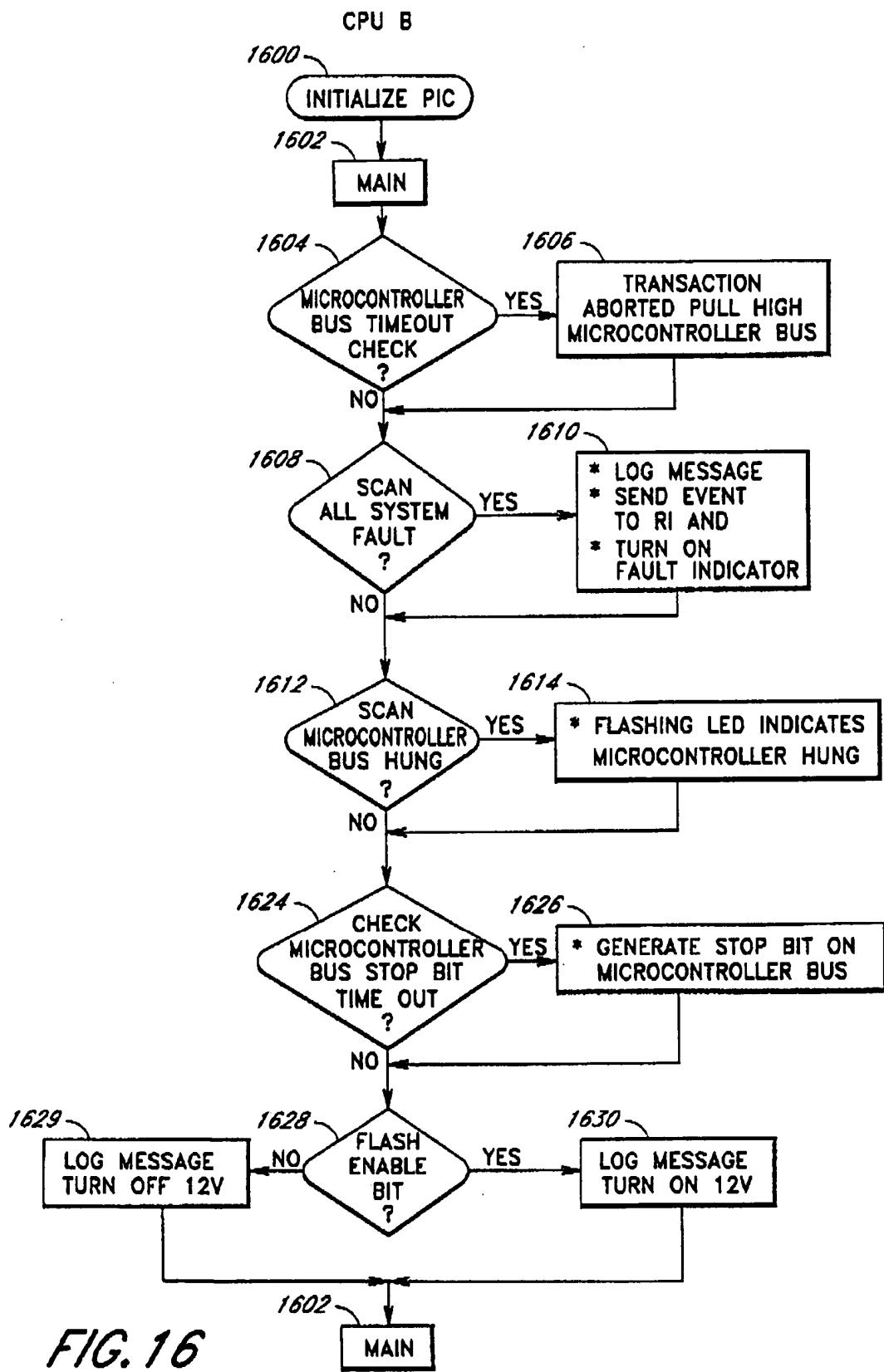


FIG. 16

03542662 - 16001457

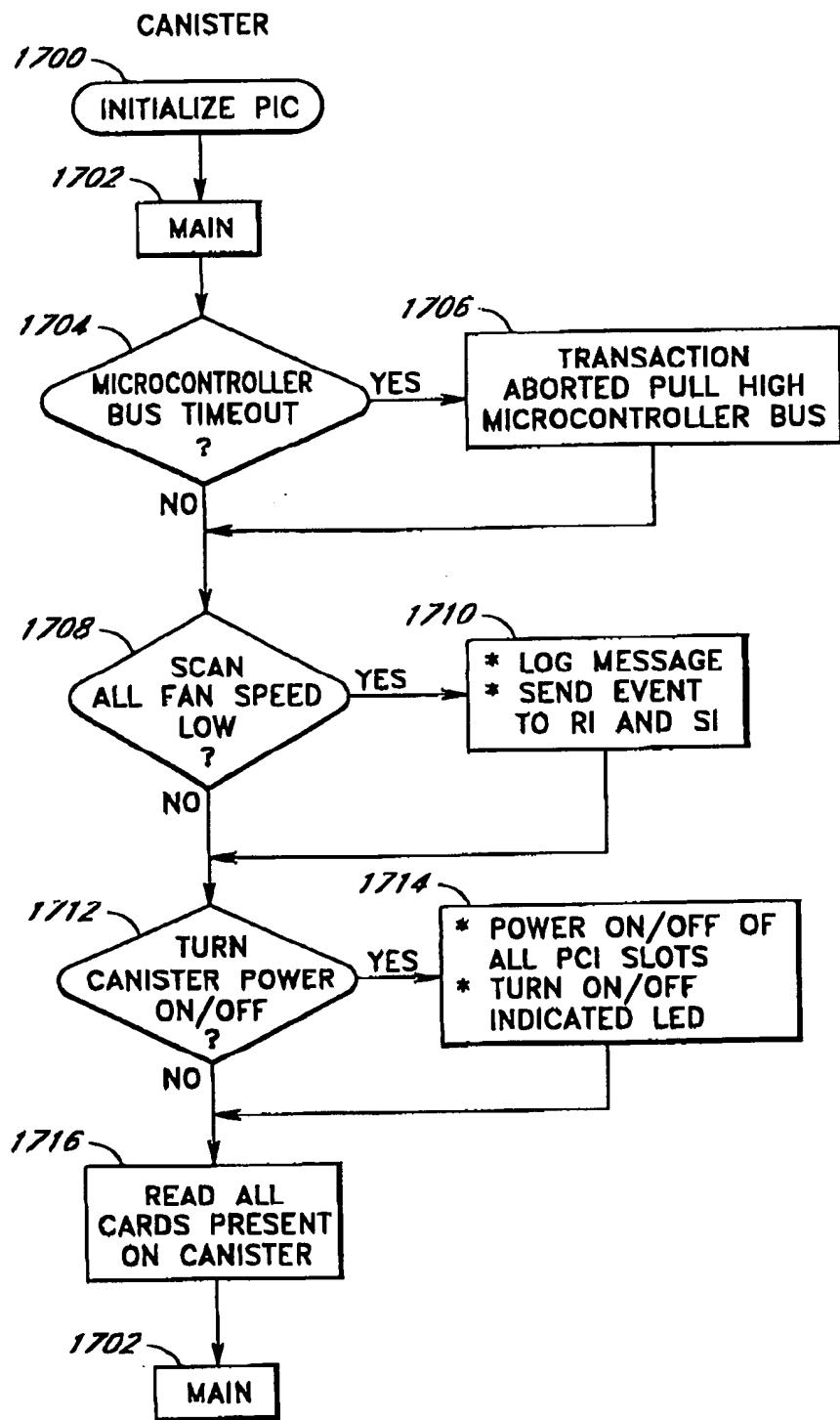


FIG. 17

SYSTEM RECORDER

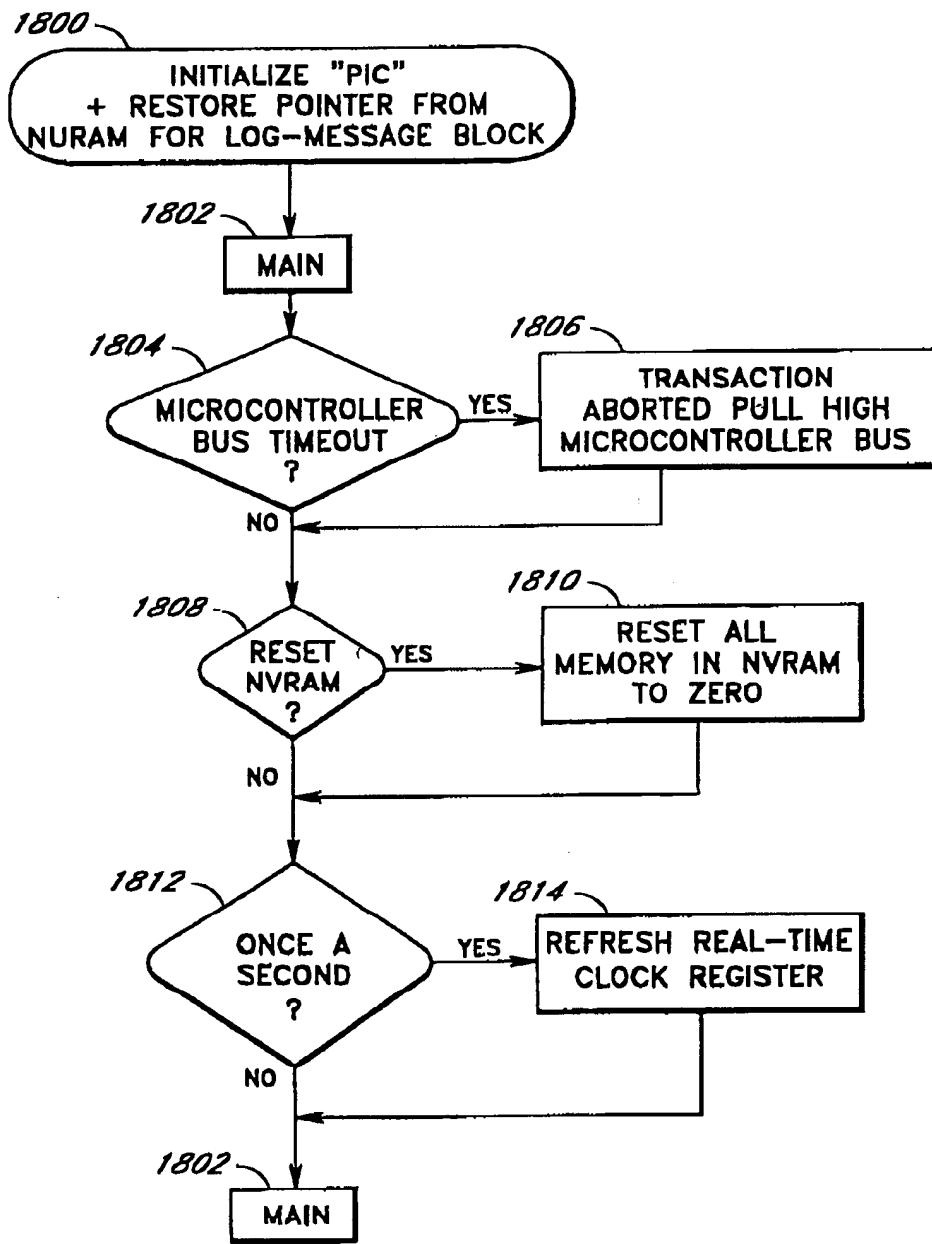


FIG. 18